



Vertical 3D Memory Technologies

Betty Prince

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The large scale integration and planar scaling of individual system chips is reaching an expensive limit. If individual chips now, and later terrabyte memory blocks, memory macros, and processing cores, can be tightly linked in optimally designed and processed small footprint vertical stacks, then performance can be increased, power reduced and cost contained. This book reviews for the electronics industry engineer, professional and student the critical areas of development for 3D vertical memory chips including: gate-all-around and junction-less nanowire memories, stacked thin film and double gate memories, terrabit vertical channel and vertical gate stacked NAND flash, large scale stacking of Resistance RAM cross-point arrays, and 2.5D/3D stacking of memory and processor chips with through-silicon-via connections now and remote links later.

Key features:

- Presents a review of the status and trends in 3-dimensional vertical memory chip technologies.
- Extensively reviews advanced vertical memory chip technology and development
- Explores technology process routes and 3D chip integration in a single reference

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